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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

ZHONGNING LIANG ET AL

Atty. Docket No.

NL 000195

Serial No. 09/829,797

Group Art Unit: 2811

Filed: APRIL 10, 2001

SEMICONDUCTOR DEVICE

Honorable Commissioner of Patent and Trademarks
Washington, D.C. 20231

CLAIM FOR PRIORITY

Sir:

A certified copy of the European Application No. 00201315.9 filed April 12, 2000 referred to in the Declaration of the above-identified application is attached herewith.

Applicants claim the benefit of the filing date of said European application.

Respectfully submitted,

By _____
Steven R. Biren, Reg.26,531
Attorney
(914) 333-9630

Enclosure

CERTIFICATE OF MAILING

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Bescheinigung | Certificate | Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

00201315.9

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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I.L.C. HATTEN-HECKMAN

DEN HAAG, DEN
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Blatt 2 der Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

Anmeldung Nr.:
Application no.: 00201315.9
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Anmeldetag:
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Anmelder:
Applicant(s):
Demandeur(s):
Koninklijke Philips Electronics N.V.
5621 BA Eindhoven
NETHERLANDS

Bezeichnung der Erfindung:
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Titre de l'invention:
Semiconductor device

In Anspruch genommene Priorität(en) / Priority(ies) claimed / Priorité(s) revendiquée(s)

Staat: State: Pays:	Tag: Date: Date:	Aktenzeichen: File no. Numéro de dépôt:

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Semiconductor device.

The present invention relates to the field of semiconductor devices and more specifically to integrated circuits (ICs) having bond pads incorporated therein. More particularly, the invention relates to a semiconductor device comprising a new bond pad structure wherein cracking is eliminated, or at least reduced. More in detail, the present invention relates to a semiconductor device comprising a bond pad structure, which enables wire bonding and probing to be carried out without the induction of - or at least with a reduced occurrence of - cracks in the intermetal dielectrics applied.

In nowadays IC technology, bond pads consist of multilayer aluminum metallization, generally with one or more layers of e.g. titanium or titanium nitride. Bond pads are present for attaching solder, wire or other bonding elements, especially constructed from aluminum, gold or copper.

Bond pads are typically disposed above one or more layers or stacks of brittle and/or soft intermetal dielectric materials, such as silicon oxides and organic materials.

Bond pad cracks can occur during ultrasonic wire bonding or even through probing. Cracks can lead to reliability problems, especially when low-k spin on dielectrics, such as hydrogen silsesquioxane (HSQ), are used. Such dielectrics, and especially HSQ, are more brittle than other oxides such as tetraethoxy silane based oxides. In HSQ layers cracks can therefore more easily propagate than in other oxides. Similar problems occur with aerogels, organic polyimides, parylenes and so on, which all have low dielectric constants as compared to silicon oxides, but are structurally and mechanically weaker than these oxides.

In the art, there is a need for structures or methods to prevent or at least reduce the occurrence of bond pad cracking.

It has been proposed in EP-A-0 875 934 to dispose a patterned reinforcing structure in a dielectric layer disposed under the bond pad. The basic principle laid down in this document is that through the use of metal grids mechanical reinforcement of the dielectric stack can be achieved and damage due to bonding can be prevented. More in detail, this known reinforced structure is manufactured by forming a metal layer, patterning the metal layer in a predetermined area into a predetermined pattern having a plurality of vacant areas and forming a dielectric layer above the patterned metal layer, filling the vacant areas in

the patterned metal layer. Finally, a bond pad is formed on the dielectric layer above the patterned metal layer.

The known reinforcing structure may be a joined or interconnected grid or cross-hatch structure with a plurality of voids or vacant areas for containing and accommodating a large portion of weak dielectric material such as the said HSQ and the like. The grid structure is planar with a thickness less than the thickness of the intermetal dielectric stack. In another embodiment the reinforcing structure includes a repeating and non-interconnected pattern such as a crucifix pattern arranged in a regular manner. Other structures such as spirals have been described as well.

The present inventors have intensively studied two of the structures known from EP-A-0 875 934:

- the cross-hatch structure, wherein at each metal level under the bond pad a cross-hatch grid of metal was inserted to confine mechanically relatively weak HSQ into square reservoirs created by the grid; and
- the crucifix structure. This structure provides a more open metal pattern as compared with the cross-hatch structure, allowing HSQ to flow more easily into the voids.

In the cross-hatch structure, the metal linewidths and spacings were designed to confine much of the HSQ into the reservoirs while minimizing the area of each reservoir, so that the HSQ layer is spared in direct mechanical impact of bonding. Vias were formed only at the pad periphery.

In the crucifix structure, the more open pattern allows the HSQ the flow more easily in the voids present in the structure. This reduces the amount of HSQ remaining over the metal lines somewhat further as compared to the cross-hatch structure.

Both known structures have however a TEOS dielectrics layer of full bond pad between the metal layers, which dielectrics can be cracked due to bonding or probing.

The present invention aims to solve or at least reduce this problem.

In accordance with the present invention, it has now been found that elimination, or at least reduction of bond pad cracking can be achieved by isolating the intermetal dielectrics with metal lines and via lines. Further, the bond pad structure of the semiconductor device according to the present invention prevents the propagation of any cracks that are formed. Moreover, metal peal off during bonding is diminished. Metal peal off is a failure mode occurring at the interface between a top metal plate and intermetal dielectrics.

More in detail, the present invention is based on the principle that use is made of via lines together with metal lines to completely isolate intermetal dielectrics. Thereto, the

invention relates to a semiconductor device comprising a bond pad structure, which bond pad structure comprises a bond pad disposed above at least one layered structure, but preferably a stack of layered structures, wherein the layered structure comprises a metal layer and a layer of a dielectric material, characterized in that in the intermetal layer of dielectric material via lines are present and arranged in such a way that the metal layers and the via lines form isolated areas filled with the dielectric material.

Furthermore, the present invention relates to a method of manufacturing a semiconductor device as described above, which method comprises the steps of:

(a) forming a metal layer;

(b) forming a dielectric layer;

(c) patterning via lines or grids in the dielectric layer;

(d) filling the patterned via grids with a conductive material, such as a metal, and preferably tungsten or copper; and

(e) applying on top of the dielectric layer and via grids formed a metal bond pad.

By the use of via lines connected to the metal layer, the adhesion between the top metal plate and the underlying layers is enhanced, so that metal peal off occurs no longer or less often.

Without wishing to be bound to a very specific theory, it is assumed that when a crack is formed in an intermetal dielectric, the system releases elastic energy and gains surface energy. Based on thermodynamic principles, the crack should not form when the elastic energy to be released is less than the surface energy to be gained. Since elastic energy is proportional with the volume of the dielectric and surface energy is proportional with the surface area of the dielectric, the present invention makes use of a small volume-to-area ratio by using small feature sizes. Therefore, the via lines, or optionally the via grids are advantageously arranged in such a way that the volume-to-surface area is - dependent on the dielectric material used - adjusted such that the elastic energy to be released on crack forming is less than the surface energy to be gained on crack forming.

Apart from the above, it is noted that in the art vias are normally patterned in squared or round pillars. Multiple rows of such pillars, shifted with respect to each other, are in use in e.g. seal rings to prevent the propagation of cracks. However, in accordance with the present invention via lines, e.g. in the form of a via grid, avoid the formation of cracks as well as the propagation in case a crack is formed anyway. Moreover, bonding stress can be released by ductile properties of the via-metal, in particular when using tungsten as via-metal.

The present invention will be described in further detail while referring to the drawings, wherein

Fig. 1 is a schematic top view of the bondpad structure of the semiconductor device according to the invention;

Figs. 2 and 3 are cross-sections of two embodiments of the bondpad structure of the semiconductor device of the present invention, wherein the upper cross-sections of Figs. 2 and 3 are cross-sections of the structure of Fig. 1 indicated with the upper arrow, while the lower cross-sections of Figs. 2 and 3 are cross-sections of the structure of Fig. 1 indicated with the lower arrow.

Fig. 1 shows a schematic top view of the bond pad structure of the semiconductor device of the present invention at via level. This top view shows the cross-hatch feature of the structures. Intermetal dielectrics are isolated by metal and via lines. The details will become clear from Figs. 2 and 3.

In Fig. 2, an embodiment is shown wherein each layered structure comprises a metal plate 1. Intermetal dielectrics 4 are isolated by two adjacent metal plates 1 and in vertical direction by via lines or grids 3. Thereto via lines of e.g. tungsten are applied on the metal plates, after which a dielectric material is applied in a manner known per se, e.g. in the manner as described in the above-mentioned EP-A-0 875 934.

Fig. 3 shows the embodiment wherein the top and bottom layered structures comprise a metal plate 1, while the intermediate layered structures are formed by metal lines or grids 2. Intermetal dielectrics 4 are isolated by the top and bottom metal plates 1 and by the metal lines 2 and via lines 3 in between.

The distances between the via lines or via grids in a particular layer structure are chosen such that the volume-to-surface area ratio of the dielectrics 4 in the direction parallel to the bond pad is sufficiently small to prevent crack forming during probing or bonding. For example, when the dielectrics thickness is 1 μm, then the width and length of the dielectric block should be smaller than 10 μm. Normally, a bond pad size is about 80 x 80 μm. Without the isolation of the dielectric layers cracks can easily form.

On top of the structures in accordance with the invention a bond pad, preferably of Al, is applied.

CLAIMS:

1. A semiconductor device comprising a bond pad structure, which bond pad structure comprises a bond pad disposed above at least one layered structure, but preferably a stack of layered structures, wherein the layered structure comprises a metal layer and a layer of a dielectric material, characterized in that in the intermetal layer of dielectric material via lines are present and arranged in such a way that the metal layers and the via lines form isolated areas filled with the dielectric material.

2. A semiconductor device as claimed in claim 1, wherein the via lines are lines of tungsten.

3. A semiconductor device as claimed in claim 1 or 2, wherein a stack of layered structures is present.

4. A semiconductor device as claimed in claim 3, wherein the metal layer in each layered structure is a metal plate.

5. A semiconductor device as claimed in claim 4, wherein the top and bottom metal layer of the stack are metal plates, and the intermediate metal layer or layers are parallel metal lines.

6. A semiconductor device as claimed in any one of the preceding claims, wherein the via lines and/or metal lines are patterned in the form of a grid.

7. A method of manufacturing a semiconductor device as claimed in any one of the preceding claims comprising the steps of:

(a) forming a metal layer;

(b) forming a dielectric layer;

(c) patterning via lines or grids in the dielectric layer;

(d) filling the patterned via grids with a conductive material, such as a metal, and preferably tungsten or copper; and

(e) applying on top of the dielectric layer and via grids formed a metal bond pad.

8. A method as claimed in claim 7, wherein following step (d) steps (a), (b), (c) and (d) are at least one time repeated.

9. A method as claimed in claim 7, wherein following step (d), lines of metal are formed, followed by steps (b), (c) and (d).

10. A method as claimed in any one of claims 7 to 9, wherein the via lines or lines of metal are applied in the form of a grid.

ABSTRACT:

The invention relates to a semiconductor device comprising a bond pad structure, which bond pad structure comprises a bond pad disposed above at least one layered structure, but preferably a stack of layered structures, wherein the layered structure comprises a metal layer and a layer of a dielectric material. In the intermetal layer of dielectric material via lines are present and arranged in such a way that the metal layers and the via lines form isolated areas filled with the dielectric material.

(Fig. 3)

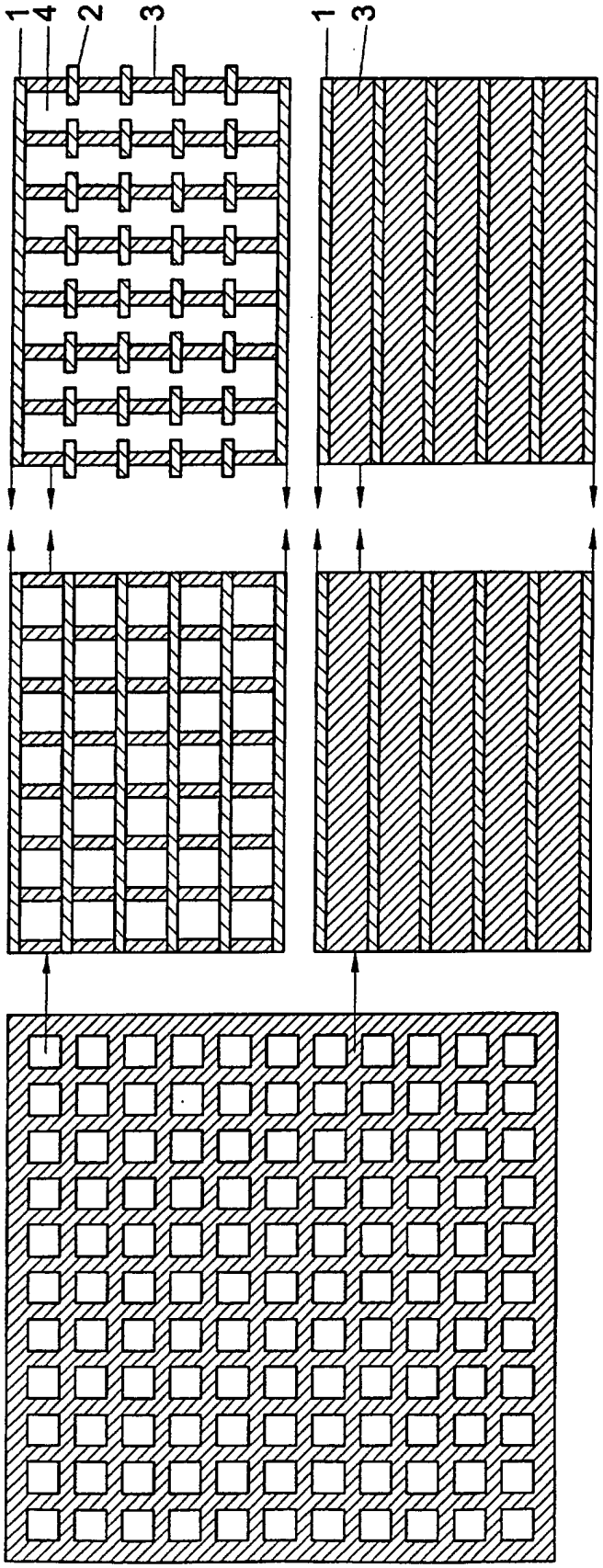

FIG. 3

FIG. 2

FIG. 1